Grenze International Journal of Engineering and Technology, July 2017

Fast Architectures for Arithmetic Operations via Vedic Sutras

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***Abstract*—The "Time" and "area" are the two important constraints in any processor IC design. In any digital design process, these two constraints play a contradictory role and thus there exists a trade-off between them. Optimizing the two said constraints is a challenging task in the design process.**
The arithmetic operations {+, - ,* $()^2$ } have been found to possess redundancy when implemented in conventional way. Based upon simulation using Vedic mathematics, resource utilization and time delay will reduce by more than 50% to 75% for multiplication and squaring with increase in number of digits.
This paper presents Vedic mathematical based arithmetic operation implementation and the results have been presented using Urdhva Tiryagbhyam, Dvandva Yoga sutras.

***Index Terms*— VHDL code,Urdhva Tiryagbhyam, Dvandva Yoga, Viniculum, Vilokanam, Booth's algorithm, Anthyaore Dashakepi.**

I. INTRODUCTION

Conventional mathematics is an integral part of any digital computational system design.Microprocessor manufacturers have developed their computer architectures suitable for conventional binary arithmetic methods. Most of the computations are inherently built using the conventional arithmetic approaches, which are mostly monotonous, shift and macro-based (repeated usage). Such approaches generally pose many limitations such as exhibiting speed limitations, excessive resource utilization in the processor, ending up in fatigue and stress experienced by users.
The Vedic mathematics approach is choice based and considered very close to the way human brain works. In the present work two generalized sutras, viz, urdhva-tiryagbham and dvandva yoga for multiplication and squaring operations respectively are implemented. The work emphasizes the hierarchical approach used to develop the higher digital systems using the cascaded single digit block architecture.

II. VEDIC APPROACH FOR ARITHMETIC OPERATIONS

A. Shudha

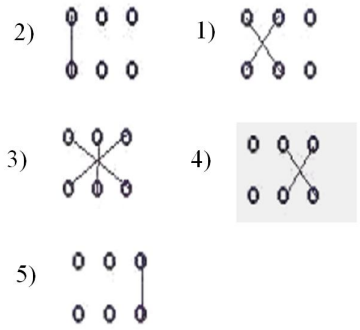
Addition in Vedic approach is performed using Shudha which is similar to place wise addition .In this method when the sum of two digits equals 10 it is represented by shudha (dot). The exceeding number is used for further operation. This process to be faster by the human observation (vilokanam) rather than computer.[1]

Grenze ID: 01.GIJET.3.3.96

B. Urdhva–tiryagbhyam

It is the general formula applicable to all cases of multiplication. The formula itself is very short and terse, consisting of only one compound word and means "vertically and crosswise". The application of this sutra will ensure simpler means to solve typical multiplication problems encountered in the engineering environment.[1]

Flow diagram for 3 digit multiplication



The result of 3 digit multiplication consists of these 5 parts from left to right

C. Dvandva yoga for squaring

In order to calculate the square of a number, 'duplex' property has been proposed. In the duplex, we take twice the product of the outermost pair, and so on till no pairs are left. When there are odd numbers of bits in the original sequence there is one digit left by itself in the middle, and this enters as such, thus For a 1 digit number, D is square of the number i.e., D (a)=a^2;[1]

For a two digit number D is twice as their product, D (ab) =2*a*b;

For a three-digit number D is twice the product of the outer pair and square of the middle digit. D (abc) =2*a*c+b^2;

For a four digit number D is twice the product of the outer pair plus twice the product of the inner pair, i.e. D (abcd) =2*a*d+2*b*c

D. Anthyaore Dashakape

This Sutra is used when the sum of unit's digit is 10 .This sutra based on the human observation (vilokanam)

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    9 2
    9 8
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9*(9+1) |  2*8   = 9016
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III. VHDL IMPLEMENTATION FOR VEDIC SUTRAS

In this study, the algorithms are implemented on VHDL and logic simulations are done on Model Simulator. The Synthesis is done using Xilinx 9.2i. The low level designs for 8 bit operations were derived from the VHDL codes, which were made to ape the Vedic algorithms. The algorithms were extracted out of proper studies of the Vedic methods and were optimized to the level of implementation.

The higher systems were developed from the so got low level 8-bit systems using the concept of port map. Thus, in case of multiplication, all the designed systems followed the same architecture as shown in the figure 1. The depicted architecture for multiplication houses three adders and four instances of lower level multiplier components, i.e., and one 16 bit adder architecture involves three adders and four 8 bit multiplier components. This trend follows for any higher level systems.

So is the case with the squaring systems. Typical architecture shown in the figure2 portrays the organization of the lower level systems in developing the higher ones. For e.g. The 16 bit squaring architecture houses three adders, two low levels, say, 8 bit squaring blocks and one 8 bit multiplier block relying on the

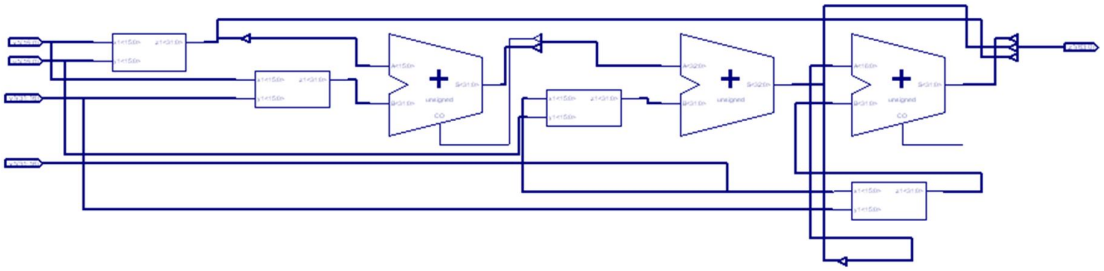

Figure 1. proposed architecture for N bit multiplication

urdhavtiryagbhaym sutra for its operation. The same architecture can be effectively used in the development of any higher level systems.

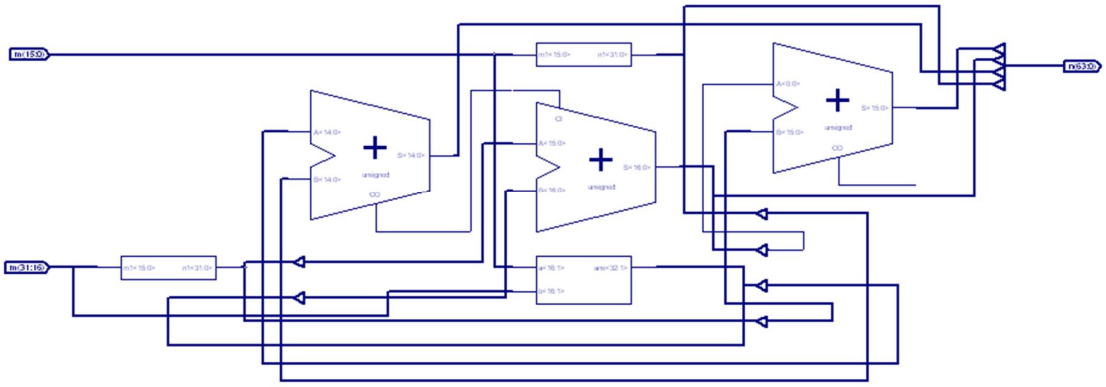

Figure 2. proposed architecture for N bit squaring

IV. RESULTS

Port map concept available in the VHDL literature was exploited to make possible, the implementation of the designs. The concept of port map abridges the low level design modules with the higher ones without the loss of generality involved in the design process.[4,5]

The time constraint and the area constraints are the two targeted constraints. The area constraint necessarily depicts the amount of area consumed by the system in terms of ”cell usage” and the time constraints speaks of the maximum combinational path delay encountered in the system. The designs were built so effectively that they promise the necessary optimization required for the practical implementations. Typical comparison tables shown below summarize the essence and the beauty of the Vedic procedures. The proposed Vedic method for multiplication was compared with the traditional method of multiplications in terms of area and time constraints and the proposed squaring designs were compared with the respective systems developed on the basis of Flynn’s algorithms.[2,3]

TABLE I: COMPARISON OF TRADITIONAL METHODS WITH THE PROPOSED URDHVA TIRYAG BHYAM METHOD FOR MULTIPLICATION

Name of multiplier		Vendor	Device Family & Device	Package	Speed Grade	Cell Use	Estimated Delay (ns)
Conventional Method of multiplication	8 X 8 bit	Xilinx	Virtex E XCV300e	BG432	-8	224	13.174
	16 X 16	Xilinx	Virtex E XCV300e	BG432	-8	916	16.380
Proposed VEDIC Method of multiplication	8 X 8 bit	Xilinx	Virtex E XCV300e	BG432	-8	16	7.793
	16 X 16	Xilinx	Virtex E XCV300e	BG432	-8	147	15.967

TABLE II: COMPARISON OF THE PROPOSED SQUARING SYSTEM CONSTRAINTS WITH THE SYSTEM CONSTRAINTS DEVELOPED BY FLYNN

Name of multiplier		Vendor	Device Family & Device	Package	Speed Grade	Cell Use	Estimated Delay (ns)
Square Proposed by Flynn	8 X 8 bit	Xilinx	Virtex E XCV300e	BG432	-8	177	30.370
	16 X 16	Xilinx	Virtex E XCV300e	BG432	-8	727	60.646
Proposed square	8 X 8 bit	Xilinx	Virtex E XCV300e	BG432	-8	32	8.728
	16 X 16	Xilinx	Virtex E XCV300e	BG432	-8	135	16.127

V. CONCLUSION

The effective implementation of these sutras can be made possible with the support of suitable architectures, using VLSI technologies available in the literature. A tremendous change in technology can be foreseen when these sutras are implemented in Design of ALU, VLSI, DSP, and Microprocessor
Vedic mathematics is a powerful approach if complementing and viniculum is given scope for hardware for which the need arises to think about 5 bit register for each digit instead of 4 bit in conventional way. In future 5 bit register will create a break through in near future using Vedic sutras for fast computation.

ACKNOWLEDGEMENTS

Our sincere and heart felt thanks to Prof. Shriram Chouthaiwale, from Yawatmal, Maharashtra and Dr. Ramesh Kolluru, Art Of Living Ashram, Bangalore for initiating us into Vedic Mathematics.

REFERENCES

[1] Jagadguru Swami Sri Bharati Krishna Tirthaji Maharaja, "Vedic mathematics," Motilal Banarsidass Publishers Pvt Ltd, Delhi 2001.
[2] P Chidgupkar and M T Karad:" Implementation of Vedic Algorithms in DSP," Global J of Engg. Educ., vol 8, no 2, published in Australia 2004 UICEE.
[3] Dr. Subhash Kulkarni, "VHDL implementation of vedic sutras"IEEE sponcered ICSIP,DEC 2006,Hubli.
[4] Douglas L. Perry:"VHDL," 3 editions, Mc Graw-Hill. 1999.
[5] J. Bhaskar:"A VHDL Primer," Pearson Education.3 Edition.2005.